

## 6.5-V TO 28-V INPUT VOLTAGE, 5-V FIXED OUTPUT, 2-A OUTPUT CURRENT, NON-SYNCHRONOUS STEP-DOWN REGULATOR WITH INTEGRATED MOSFET

Check for Samples: [TPS5405](#)

### FEATURES

- Fixed 5-V Output
- 6.5-V to 28-V Wide Input Voltage Range
- Up to 2-A Maximum Continuous Output Loading Current
- Pulse Skipping Mode to Achieve High Light Load Efficiency
- Over 80% Efficiency at 10-mA Loading
- Adjustable 50-kHz to 1.1-MHz Switching Frequency Set by an External Resistor (Leave pin ROSC floating. Set frequency to 120 kHz)
- Peak Current-Mode Control
- Cycle-by-Cycle Over Current Protection
- Switching Node Anti-Ringing to Ease EMI Issue
- External Soft Start
- Available in SOIC8 Package

### APPLICATIONS

- 9-V, 12-V and 24-V Distributed Power Systems
- Consumer Applications Such as Home Appliances, Set-Top Boxes, CPE Equipment, LCD Displays, Peripherals, and Battery Chargers
- Industrial and Car Entertainment Power Supplies

### DESCRIPTION

The TPS5405 is a monolithic non-synchronous buck regulator with wide operating input voltage range from 6.5 V to 28 V. Current mode control with internal slope compensation is implemented to reduce component count.

TPS5405 also features a light load pulse skipping mode, which allows for a power loss reduction from the input power supply to the system at light loading.

The switching frequency of the converters can be set from 50 kHz to 1.1 MHz with an external resistor. Frequency spread spectrum operation is introduced for EMI reduction.

LX anti-ringing is added to address high frequency EMI issues.

A cycle-by-cycle current limit with frequency fold back protects the IC at over loading condition.



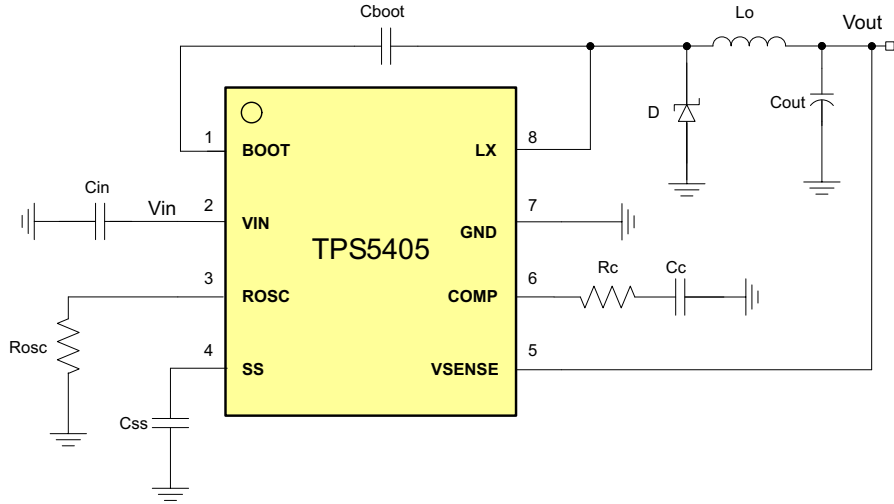
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



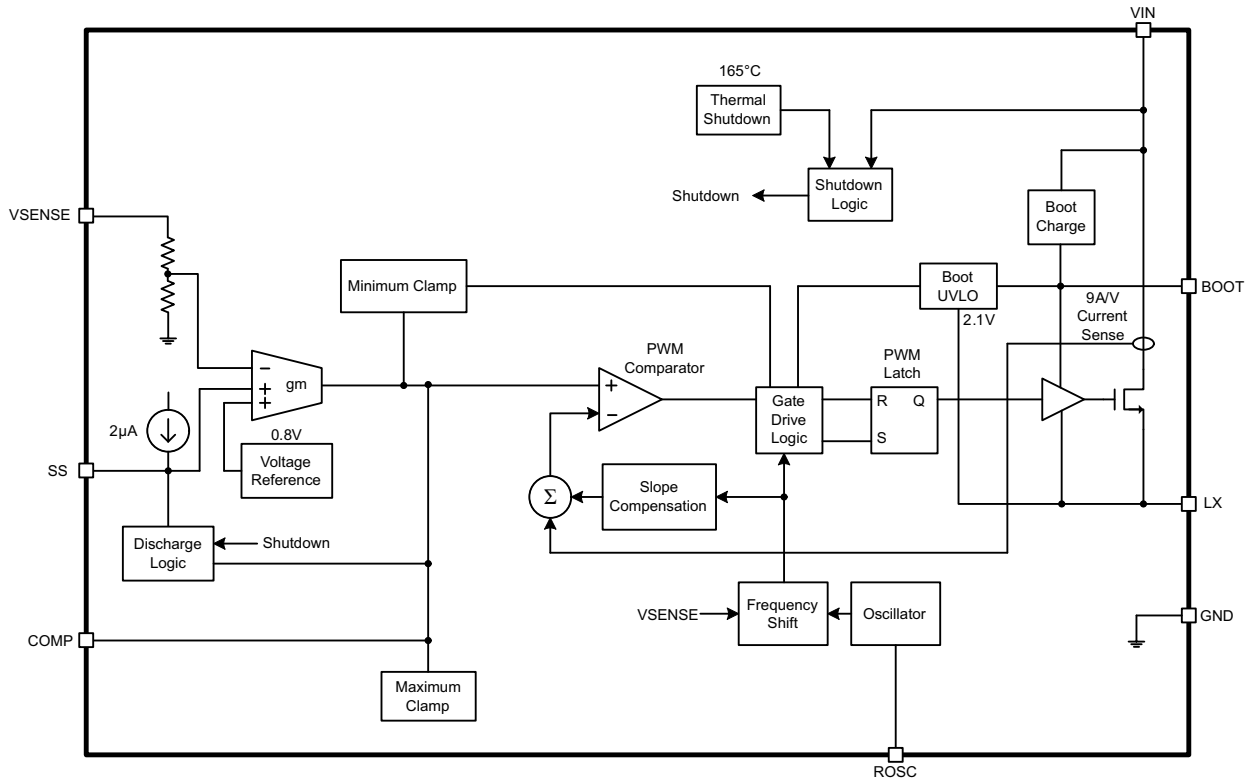
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

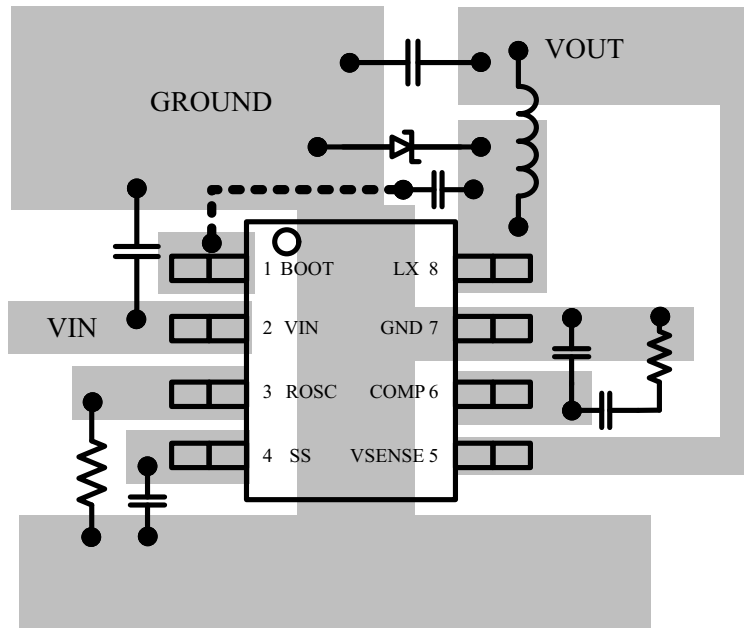
### TYPICAL APPLICATION



### FUNCTIONAL BLOCK DIAGRAM



### PCB LAYOUT

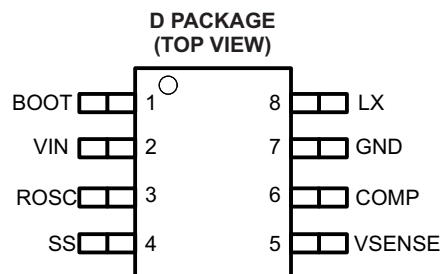


### ORDERING INFORMATION<sup>(1)</sup>

T <sub>A</sub>	PACKAGE <sup>(2)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	8-pin SOIC (D)	TPS5405DR	T5405

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).  
 (2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

### PIN OUT



### TERMINAL FUNCTIONS

NAME	NO.	DESCRIPTION
BOOT	1	A 0.1- $\mu$ F bootstrap capacitor is required between BOOT and LX.
VIN	2	Input supply voltage, 6.5 V to 28 V
ROSC	3	Switching frequency program pin. Connect a resistor to this pin to set the switching frequency. Leave the pin open for 120-kHz switching frequency.
SS	4	Soft start pin. An external capacitor connected to this pin sets the output rise time.
VSENSE	5	Output voltage feedback pin
COMP	6	Error amplifier output and input to the PWM comparator. Connect frequency compensation components to this pin.
GND	7	Ground
LX	8	Switching node to external inductor

## ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

	Voltage range at VIN, LX	–0.3 to 30	V
	Voltage range at LX (maximum withstand voltage transient < 20 ns)	–5 to 30	V
	Voltage from BOOT to LX	–0.3 to 7	V
	Voltage at VSENSE	–0.3 to 7	V
	Voltage at SS	–0.3 to 3	V
	Voltage at ROSC	–0.3 to 3	V
	Voltage at COMP	–0.3 to 3	V
	Voltage at GND	–0.3 to 0.3	V
T <sub>J</sub>	Operating junction temperature range	–40 to 125	°C
T <sub>STG</sub>	Storage temperature range	–55 to 150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Input operating voltage	6.5		28	V
T <sub>A</sub>	Ambient temperature	–40		85	°C

## THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		TPS5405	UNITS
		D	
		8 PINS	
θ <sub>JA</sub>	Junction-to-ambient thermal resistance <sup>(2)</sup>	116.7	°C/W
θ <sub>JCtop</sub>	Junction-to-case (top) thermal resistance <sup>(3)</sup>	62.4	
θ <sub>JB</sub>	Junction-to-board thermal resistance <sup>(4)</sup>	57.0	
ψ <sub>JT</sub>	Junction-to-top characterization parameter <sup>(5)</sup>	14.5	
ψ <sub>JB</sub>	Junction-to-board characterization parameter <sup>(6)</sup>	56.5	
θ <sub>JCbot</sub>	Junction-to-case (bottom) thermal resistance <sup>(7)</sup>	N/A	

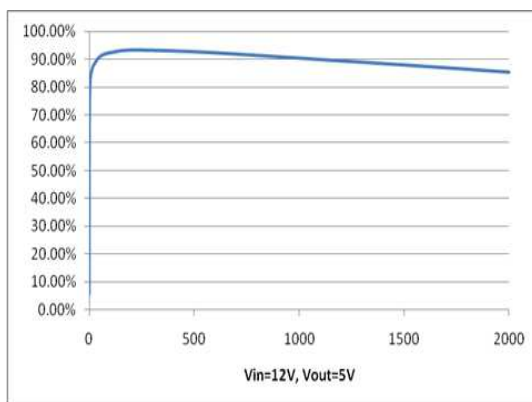
- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter, ψ<sub>JT</sub>, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ<sub>JA</sub>, using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter, ψ<sub>JB</sub>, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ<sub>JA</sub>, using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

## ELECTRICAL CHARACTERISTICS

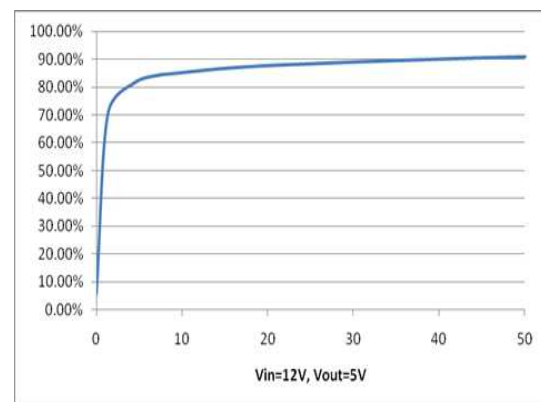
 $T_A = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{IN} = 12\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>INPUT SUPPLY</b>						
$V_{IN}$	Input Voltage range	VIN1 and VIN2	6.5		28	V
$I_{DDQ\_nsw}$	Non switching quiescent power supply current	VFB1 = VFB2 = 900 mV, LOW_P = high		100		$\mu\text{A}$
$UVLO$	$V_{IN}$ under voltage lockout	Rising $V_{IN}$		3.5		V
		Hysteresis		200		mV
<b>FEEDBACK AND ERROR AMPLIFIER</b>						
$V_{SENSE}$	Regulated output voltage	$V_{IN} = 12\text{ V}$	4.85	5	5.15	V
$G_{m\_EA}$	Error amplifier trans-conductance	$-2\ \mu\text{A} < I_{COMP} < 2\ \mu\text{A}$ , $V_{COMP} = 1\text{ V}$		92		$\mu\text{s}$
$I_{gm}$	Error amplifier source/sink current	$V_{COMP} = 1\text{ V}$ , 100 mV overdrive		$\pm 7$		$\mu\text{A}$
$G_{m\_SRC}$	COMP voltage to inductor current Gm	$V_{IN} = 12\text{ V}$		9		A/V
<b>PFM MODE AND SOFT-START</b>						
$I_{th}$	Pulse skipping mode switch current threshold			300		mA
$I_{SS}$	Charge current			2		$\mu\text{A}$
<b>OSCILLATOR</b>						
$f_{SW\_BK}$	Switching frequency range	Set by external resistor ROSC	50		1100	kHz
$f_{SW}$	Programmable frequency	ROSC = OPEN		120		kHz
		ROSC = 85.5 k $\Omega$		300		
$f_{jitter}$	Frequency spread spectrum in percentage of $f_{SW}$	$V_{IN} = 12\text{ V}$		$\pm 6$		%
$f_{swing}$	Jittering swing frequency in percentage of $f_{SW}$	$V_{IN} = 12\text{ V}$		1/512		
$t_{min\_on}$	Minimum on time	$V_{IN} = 12\text{ V}$ , $T_A = 25^{\circ}\text{C}$		200		ns
$D_{max}$	Maximum duty ratio	$V_{IN} = 12\text{ V}$		93		%
<b>CURRENT LIMIT</b>						
$I_{LIMIT}$	Peak inductor current limit	$V_{IN} = 12\text{ V}$		2.5		A
<b>MOSFET ON-RESISTANCE</b>						
$R_{dson\_HS}$	On resistance of high side FET	$V_{IN} = 12\text{ V}$		120	240	m $\Omega$
<b>THERMAL SHUTDOWN</b>						
$T_{TRIP}$	Thermal protection trip point	Rising temperature		165		$^{\circ}\text{C}$

## TYPICAL CHARACTERISTICS

 $T_A = 25^{\circ}\text{C}$ ,  $V_{IN} = 12\text{ V}$ ,  $f_{SW} = 120\text{ kHz}$  (unless otherwise noted)


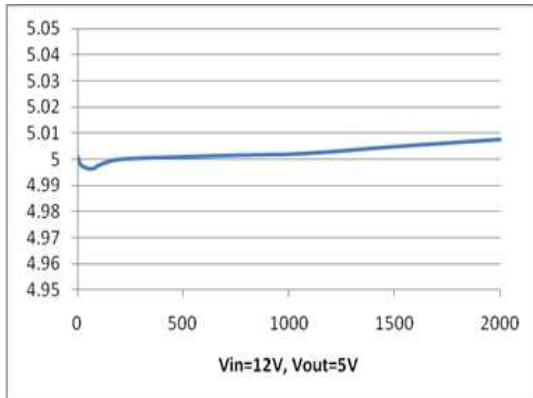
**Figure 1. Efficiency**  
 $V_{IN} = 12\text{ V}$ ,  $V_{OUT} = 5\text{ V}$



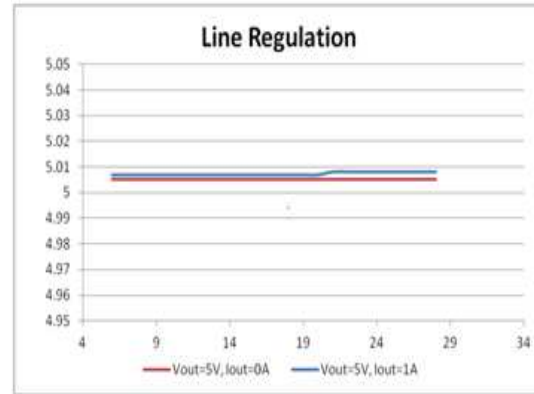
**Figure 2. Efficiency**  
 $V_{IN} = 12\text{ V}$ ,  $V_{OUT} = 5\text{ V}$

**TYPICAL CHARACTERISTICS (continued)**

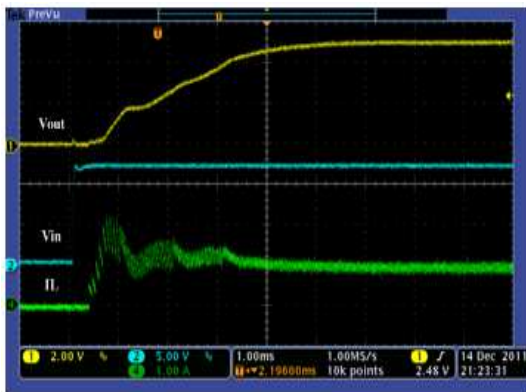
$T_A = 25^\circ\text{C}$ ,  $V_{IN} = 12\text{ V}$ ,  $f_{SW} = 120\text{ kHz}$  (unless otherwise noted)



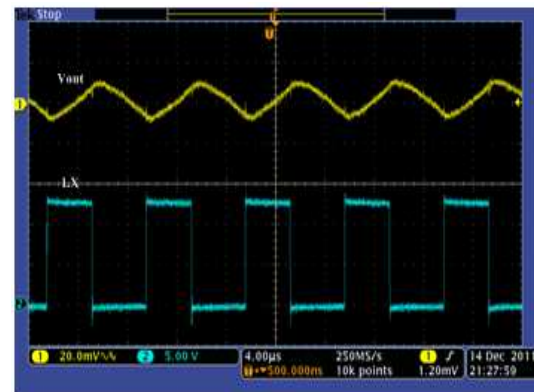
**Figure 3. Load Regulation**  
 $V_{IN} = 12\text{ V}$ ,  $V_{OUT} = 5\text{ V}$



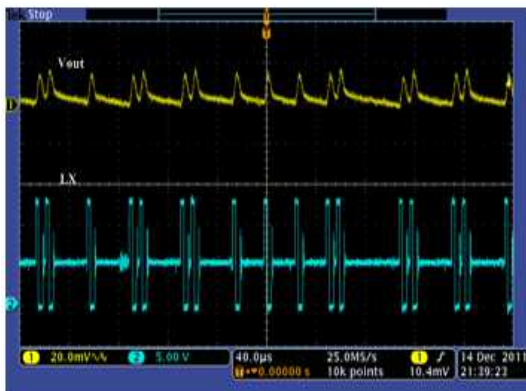
**Figure 4. Line Regulation**  
 $V_{OUT} = 5\text{ V}$



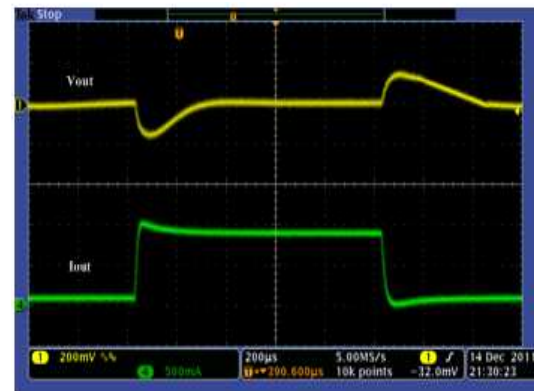
**Figure 5. Startup**  
1-A Preset Loading



**Figure 6. Steady State**  
 $I_O = 1\text{ A}$



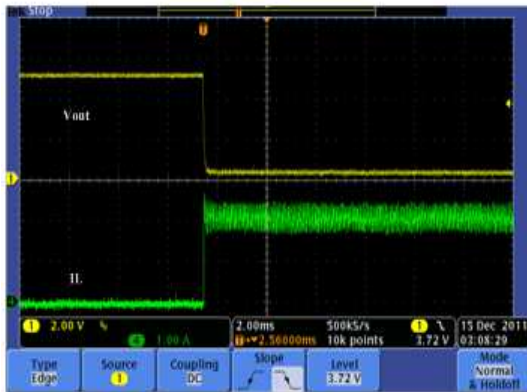
**Figure 7. Steady State**  
 $I_O = 20\text{ mA}$



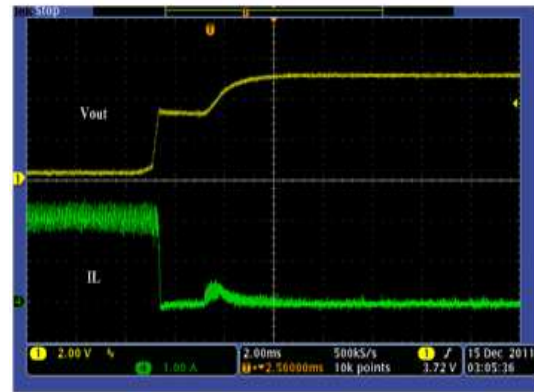
**Figure 8. Load Transient**  
 $I_O = 0.1\text{ A to }1\text{ A}$

**TYPICAL CHARACTERISTICS (continued)**

$T_A = 25^\circ\text{C}$ ,  $V_{IN} = 12\text{ V}$ ,  $f_{SW} = 120\text{ kHz}$  (unless otherwise noted)



**Figure 9. Short Circuit Protection**



**Figure 10. Short Circuit Recovery**

## OVERVIEW

The TPS5405 is a 28-V, 2-A, step-down (buck) converter with an integrated high-side N-channel MOSFET. To improve performance during line and load transients, the device implements a constant frequency, current mode control which reduces output capacitance and simplifies external frequency compensation design.

The TPS5405's switching frequency is adjustable with an external resistor or fixed by connecting the frequency program pin to GND or leaving it unconnected.

The TPS5405 starts switching at  $V_{IN}$  equal to 3.5 V. The operating current is 100  $\mu$ A typically when not switching and under no load. When the device is disabled, the supply current is 1  $\mu$ A typically.

The integrated 120-m $\Omega$  high-side MOSFET allows for high efficiency power supply designs with continuous output currents up to 2 A.

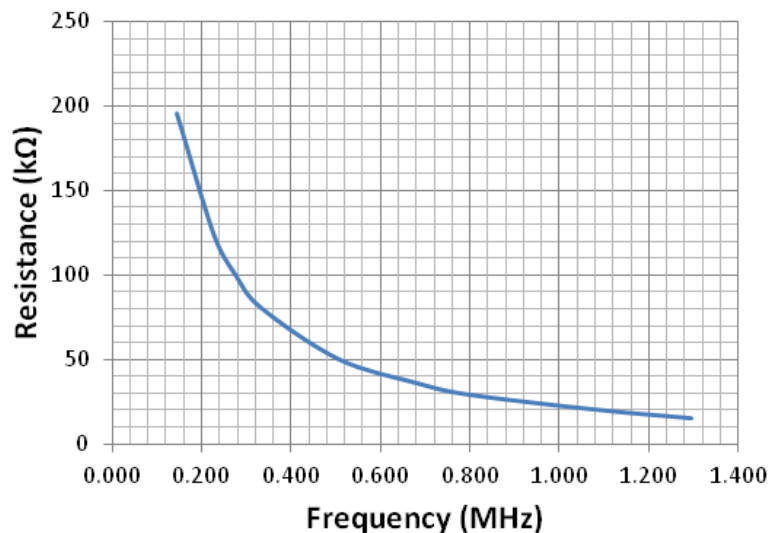
The TPS5405 reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high-side MOSFET is supplied by an external capacitor on the BOOT to PH pins. The boot capacitor voltage is monitored by an UVLO circuit and will turn the high-side MOSFET off when the voltage falls below a preset threshold of 2.1 V typically.

By adding an external capacitor, the slow start time of the TPS5405 can be adjustable which enables flexible output filter selection. To improve the efficiency at light load conditions, the TPS5405 enters a special pulse skipping mode when the peak inductor current drops below 300 mA typically. The frequency foldback reduces the switching frequency during startup and over current conditions to help control the inductor current. The thermal shut down gives the additional protection under fault conditions.

## DETAILED DESCRIPTION

### Adjustable Frequency PWM Control

The TPS5405 uses an external resistor to adjust the switching frequency. Connecting the ROsc pin to ground fixes the switching frequency at 70 kHz. Leave this pin open to set 120-kHz switch frequency.



**Figure 11. ROsc vs Switching Frequency**

$$R_{OSC}(k\Omega) = 21.82 \cdot f_{SW}^{-1.167} \quad (1)$$

For operation at 300 kHz, an 85.5-k $\Omega$  resistor is required.



## Pulse Skipping Mode

The TPS5405 is designed to operate in pulse skipping mode at light load currents to boost light load efficiency. When the peak inductor current is lower than 300 mA typically, the COMP pin voltage falls to 0.5 V typically and the device enters pulse skipping mode. When the device is in pulse skipping mode, the COMP pin voltage is clamped at 0.5 V internally which prevents the high side integrated MOSFET from switching. The peak inductor current must rise above 300 mA for the COMP pin voltage to rise above 0.5 V and exit pulse skipping mode. Since the integrated current comparator catches the peak inductor current only, the average load current entering pulse skipping mode varies with the applications and external output filters.

## Voltage Reference ( $V_{SENSE}$ )

The voltage reference system produces a  $\pm 2\%$  initial accuracy voltage reference ( $\pm 4\%$  over temperature) by scaling the output of a temperature stable bandgap circuit. The typical voltage reference is designed at 0.8 V.

## Bootstrap Voltage (BOOT)

The TPS5405 has an integrated boot regulator and requires a 0.1- $\mu$ F ceramic capacitor between the BOOT and LX pins to provide the gate drive voltage for the high-side MOSFET. A ceramic capacitor with an X7R or X5R grade dielectric is recommended because of the stable characteristics over temperature and voltage. To improve drop out, the TPS5405 is designed to operate at 100% duty cycle as long as the BOOT to LX pin voltage is greater than 2.1 V typically.

## Programmable Slow Start Using SS Pin

It is recommended to program the slow start time externally because no slow start time is implemented internally. The TPS5405 effectively uses the lower voltage of the internal voltage reference or the SS pin voltage as the power supply's reference voltage fed into the error amplifier and will regulate the output accordingly. A capacitor ( $C_{SS}$ ) on the SS pin to ground implements a slow start time. The TPS5405 has an internal pull-up current source of 2  $\mu$ A that charges the external slow start capacitor. The equation for the slow start time (10% to 90%) is shown in [Equation 2](#). The internal  $V_{ref}$  is 0.8 V and the  $I_{SS}$  current is 2  $\mu$ A.

$$t_{ss}(\text{ms}) = \frac{C_{ss}(\text{nF}) \times V_{ref}(\text{V})}{I_{ss}(\mu\text{A})} \quad (2)$$

The slow start time should be set between 1 ms to 10 ms to ensure good start-up behavior. The slow start capacitor should be no more than 27 nF.

If during normal operation, the input voltage drops below the VIN UVLO threshold, or a thermal shutdown event occurs, the TPS5405 stops switching.

## Error Amplifier

The TPS5405 has a transconductance amplifier for the error amplifier. The error amplifier compares the VSENSE voltage to the internal effective voltage reference presented at the input of the error amplifier. The transconductance of the error amplifier is 92  $\mu$ A/V during normal operation. Frequency compensation components are connected between the COMP pin and ground.

## Slope Compensation

To prevent the sub-harmonic oscillations when operating the device at duty cycles greater than 50%, the TPS5405 adds a built-in slope compensation which is a compensating ramp to the switch current signal.

## Overcurrent Protection and Frequency Shift

The TPS5405 implements current mode control that uses the COMP pin voltage to turn off the high-side MOSFET on a cycle by cycle basis. Every cycle the switch current and the COMP pin voltage are compared; when the peak inductor current intersects the COMP pin voltage, the high-side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier responds by driving the COMP pin high, causing the switch current to increase. The COMP pin has a maximum clamp internally, which limits the output current.

The TPS5405 provides robust protection during short circuits. There is potential for overcurrent runaway in the output inductor during a short circuit at the output. The TPS5405 solves this issue by increasing the off time during short circuit conditions by lowering the switching frequency. The switching frequency is divided by 8, 4, 2, and 1 as the voltage ramps from 0 V to 5V on the VSENSE pin. The relationship between the switching frequency and the VSENSE pin voltage is shown in [Table 1](#).

**Table 1. Switching Frequency Conditions**

SWITCHING FREQUENCY	VSENSE PIN VOLTAGE
$f_{sw}$	$V_{SENSE} \geq 3.75 \text{ V}$
$f_{sw}/2$	$3.75 \text{ V} > V_{SENSE} \geq 2.5 \text{ V}$
$f_{sw}/4$	$2.5 \text{ V} > V_{SENSE} \geq 1.25 \text{ V}$
$f_{sw}/8$	$1.25 \text{ V} > V_{SENSE}$

## Spread Spectrum

In order to reduce EMI, TPS5405 introduces frequency spread spectrum. The jittering span is  $\pm 6\%$  of the switching frequency with 1/512 swing frequency.

## Switching Node Anti-Ringing

When the non-synchronous buck converter operates in DCM mode, the filter inductor and the parasitic capacitance in the switching node (LX) form an LC resonant circuit; due to its high Q factor, lengthy high frequency oscillation can be observed in the switching node. This ringing could cause radiated EMI issues in some systems. TPS5405 adds an anti-ringing circuit to prevent the ringing from happening, when the inductor current crosses zero and LX starts to climb up, an internal MOSFET between LX and VSENSE is turned on, providing a damping path for the resonant circuit so as to eliminate the ringing.

## Overvoltage Transient Protection

The TPS5405 incorporates an overvoltage transient protection (OVTP) circuit to minimize output voltage overshoot when recovering from output fault conditions or strong unload transients. The OVTP circuit includes an overvoltage comparator to compare the VSENSE pin voltage and internal thresholds. When the VSENSE pin voltage goes above  $109\% \times V_{ref}$ , the high-side MOSFET will be forced off. When the VSENSE pin voltage falls below  $107\% \times V_{ref}$ , the high-side MOSFET will be enabled again.

## Inductor Selection

The higher operating frequency allows the use of smaller inductor and capacitor values. A higher frequency generally results in lower efficiency because of switching loss and MOSFET gate charge losses. In addition to this basic trade-off, the effect of the inductor value on ripple current and low current operation must also be considered. The ripple current depends on the inductor value. The inductor ripple current ( $i_L$ ) decreases with higher inductance or higher frequency and increases with higher input voltage ( $V_{IN}$ ). Accepting larger values of  $i_L$  allows the use of low inductances, but results in higher output voltage ripple and greater core losses.

To calculate the value of the output inductor, use [Equation 3](#). LIR is a coefficient that represents inductor peak-to-peak ripple to DC load current. It is recommended to set LIR to 0.1 ~ 0.3 for most applications.

Actual core loss of the inductor is independent of core size for a fixed inductor value, but it is very dependent on the inductance value selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase. Ferrite designs have very low core loss and are preferred for high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. It results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate. It is important that the RMS current and saturation current ratings are not exceeding the inductor specification. The RMS and peak inductor current can be calculated from [Equation 5](#) and [Equation 6](#).

$$L = \frac{V_{IN} - V_{OUT}}{I_O \cdot LIR} \cdot \frac{V_{OUT}}{V_{IN} \cdot f_{SW}} \quad (3)$$

$$\Delta i_L = \frac{V_{IN} - V_{OUT}}{I_O} \cdot \frac{V_{OUT}}{V_{IN} \cdot f_{SW}} \quad (4)$$

$$i_{LRMS} = \sqrt{I_O^2 + \frac{\left(\frac{V_{OUT} \cdot (V_{INmax} - V_{OUT})}{V_{INmax} \cdot L \cdot f_{SW}}\right)^2}{12}} \quad (5)$$

$$I_{Lpeak} = I_O + \frac{\Delta i_L}{2} \quad (6)$$

For this design example, use  $LIR = 0.3$  and the inductor is calculated to be  $5.40 \mu\text{H}$  with  $V_{IN} = 12 \text{ V}$ . Choose  $4.7 \mu\text{H}$  value for the standard inductor and the peak to peak inductor ripple is about 34% of 1-A DC load current.

### Output Capacitor Selection

There are two primary considerations for selecting the value of the output capacitor. The output capacitors are selected to meet load transient and output ripple's requirements.

[Equation 7](#) gives the minimum output capacitance to meet the transient specification. For this example,  $L = 4.7 \mu\text{H}$ ,  $\Delta I_{OUT} = 1 \text{ A} - 0.0 \text{ A} = 1 \text{ A}$  and  $\Delta V_{OUT} = 500 \text{ mV}$  (10% of regulated 5 V). Using these numbers gives a minimum capacitance of  $1 \mu\text{F}$ . A standard 22- $\mu\text{F}$  ceramic is chosen in the design.

$$C_O > \frac{\Delta I_{OUT}^2 \cdot L}{2 \cdot V_{OUT} \cdot \Delta V_{OUT}} \quad (7)$$

The selection of  $C_O$  is driven by the effective series resistance (ESR). [Equation 8](#) calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where  $f_{SW}$  is the switching frequency,  $\Delta V_{OUT}$  is the maximum allowable output voltage ripple, and  $\Delta i_L$  is the inductor ripple current. In this case, the maximum output voltage ripple is  $50 \text{ mV}$  (1% of regulated 5 V). From [Equation 4](#), the output current ripple is  $1 \text{ A}$ . From [Equation 8](#), the minimum output capacitance meeting the output voltage ripple requirement is  $2.5 \mu\text{F}$  with 3-m $\Omega$  ESR resistance.

$$C_O > \frac{1}{8 \cdot f_{SW}} \cdot \frac{1}{\frac{\Delta V_{OUT}}{\Delta i_L} - \text{ESR}} \quad (8)$$

After considering both requirements, for this example, one 22- $\mu\text{F}$ , 6.3-V X7R ceramic capacitor with 3-m $\Omega$  ESR should be used.

### Input Capacitor Selection

A minimum 10- $\mu\text{F}$  X7R/X5R ceramic input capacitor is recommended to be added between  $V_{IN}$  and GND. These capacitors should be connected as close as physically possible to the input pins of the converters as they handle the RMS ripple current shown in [Equation 9](#). For this example,  $I_{OUT} = 1 \text{ A}$ ,  $V_{OUT} = 5 \text{ V}$ , minimum  $V_{INmin} = 9.6 \text{ V}$ , from [Equation 9](#), the input capacitors must support a ripple current of 1-A RMS.

$$I_{INRMS} = I_{OUT} \cdot \sqrt{\frac{V_{OUT}}{V_{INmin}} \cdot \frac{(V_{INmin} - V_{OUT})}{V_{INmin}}} \quad (9)$$

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using [Equation 10](#). Using the design example values,  $I_{OUTmax} = 1 \text{ A}$ ,  $C_{IN} = 10 \mu\text{F}$ ,  $f_{SW} = 300 \text{ kHz}$ , yields an input voltage ripple of  $83 \text{ mV}$ .

$$\Delta V_{IN} = \frac{I_{OUTmax} \cdot 0.25}{C_{IN} \cdot f_{SW}} \quad (10)$$

To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current must be used.

## Bootstrap Capacitor Selection

An external bootstrap capacitor connected to the BST pins supplies the gate drive voltages for the topside MOSFETs. The capacitor between BST pin and LX pin is charged through internal diode from V7V when the LX pin is low. When a high side MOSFET is to be turned on, the driver places the bootstrap voltage across the gate-source of the desired MOSFET. This enhances the top MOSFET switch and turns it on. The switch node voltage, LX, rises to V<sub>IN</sub> and the BST pin follows. With the internal high side MOSFET on, the bootstrap voltage is above the input supply:  $V_{BST} = V_{IN} + V7V$ . The selection on bootstrap capacitance is related with internal high side power MOSFET gate capacitance. A 0.047- $\mu$ F ceramic capacitor is recommended between the BST pin and LX pin for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. The capacitor should have 10-V or higher voltage rating.

## Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 165°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. Once the die temperature decreases below 165°C, the device reinitiates the power up sequence.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS5405DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	T5405	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS5405DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS5405DR	SOIC	D	8	2500	340.5	338.1	20.6



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.  
 D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.  
 E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)